Data Sheet Revision for AD5428/AD5440/AD5447

Data Sheet Specification Comparison

Rev D

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V, temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
Write Mode			
t_1	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_3	10	ns min	$\overline{CS}$ low time
t_4	10	ns min	Address setup time
t_5	0	ns min	Address hold time
t_6	6	ns min	Data setup time
t_7	0	ns min	Data hold time
t_8	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_9	7	ns min	$\overline{CS}$ min high time
Data Readback Mode			
t_{10}	0	ns typ	Address setup time
t_{11}	0	ns typ	Address hold time
t_{12}	5	ns typ	Data access time
	25	ns max	
t_{13}	5	ns typ	Bus relinquish time
	10	ns max	
Update Rate	21.3	MSPS	Consists of $\overline{CS}$ min high time, $\overline{CS}$ low time, and output voltage settling time

Rev E

Table 2. (Continued)

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_3	10	ns min	$\overline{CS}$ low time
t_4	10	ns typ	Address setup time
t_5	10	ns typ	Address hold time
t_6	6	ns min	Data setup time
t_7	0	ns min	Data hold time
t_8	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_9	7	ns min	$\overline{CS}$ min high time
Data Readback Mode			
t_{10}	0	ns typ	Address setup time
t_{11}	0	ns typ	Address hold time
t_{12}	5	ns typ	Data access time
	25	ns max	
t_{13}	5	ns typ	Bus relinquish time
	10	ns max	
Update Rate	21.3	MSPS	Consists of $\overline{CS}$ min high time, $\overline{CS}$ low time, and output voltage settling time

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Rev D

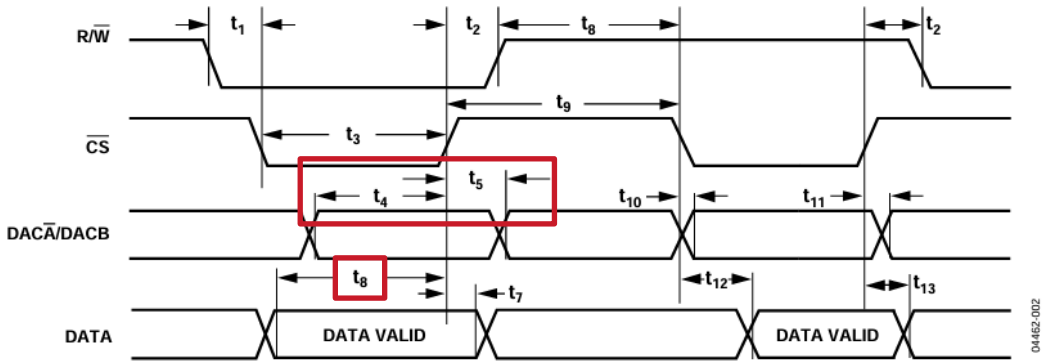

Figure 2. Timing Diagram

Rev E

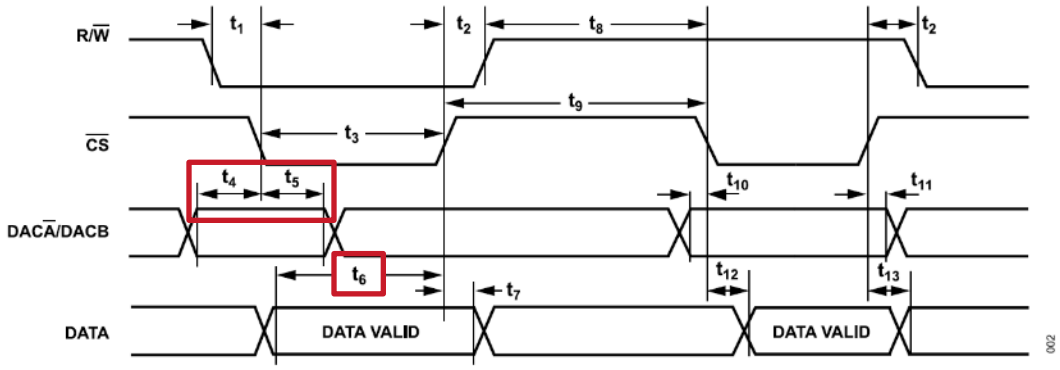

Figure 2. Timing Diagram

- T4&T5 – tested across Temp and VDD, 1 unit
- T6 change – typo fix only